

Introduction to Low Power VLSI

Introduction:-

- * Very-large scale Integration (VLSI) is the process of creating an integrated circuit (IC) by combining hundreds of thousands of transistors or devices into a single chip.
- * Design for low power has become nowadays one of the major concerns for complex, VLSI circuits.
- * micron Technology - 1 μ m, 2 μ m, 3 μ m, etc
- * Sub-micron technology - 0.8 μ m, 0.6 μ m, 0.35 μ m, 0.25 μ m etc.
- * Deep Sub-micron Technology - 0.18 μ m, 0.13 μ m.
- * Nanotechnology - 90nm, 65nm etc.

Why low power?

- * Important issues in the present day VLSI circuit realization.
 - * Increasing Transistor count
 - * Higher speed of operation
 - * Greater device leakage currents.
- * Packaging & cooling cost
 - * contemporary high performance processor consume heavy power
 - * cost associated with packaging & cooling such devices is prohibitive
 - * Low power methodology to be used to reduce cost of packaging and cooling
- * Reliability:- Every 10°C rise in temperature roughly doubles the failure rate.
- * Environment,-
 - * According to an estimate of the US Environmental Protection Agency (EPA), 80% of the power consumption by office equipment

is due to consumption equipment and a large part from unused equipment.

- * Power is dissipated in the form heat
- * The cooling techniques, such as air conditioned, transfer the heat to the environment
- * To reduce adverse effect on environment, efforts such as EPA's energy star program leading to power management standard for desktop and laptops has emerged.

Need for Low power circuit Design.

The increasing prominence of portable systems and the need to limit power consumption in very-high density VLSI chips have led to rapid innovation developments in low-power design during the recent years.

The limited battery lifetime typically impose very strict demands on the overall power consumption of the portable system. Although new rechargeable battery types such as Nickel, Metal Hydride (NiMH) are being developed with higher energy capacity than that of the conventional Nickel-Cadmium (NiCd) batteries the energy density offered new batteries technologies is about 30 watt-hour/pound.

The need for low power design is also becoming a major issue in high-performance digital systems, such as microprocessors, digital signal processors (DSPs) and other application. Increasing chip density and high operating speed lead to the design of very complex chips with high clock frequencies. If clock frequency of chip increases then power dissipation of chip thus the chip temperature increases linearly.

since the dissipated power heat must be removed effectively to keep the chip temperature cost of packaging, cooling and heat removal becomes a significant factor.

ULSI reliability is yet another concern it need for low-power design. There is a close correlation between the peak power dissipation of digital circuit and reliability problems such as electromigration and hot-carrier induced device degradation.

Source of power dissipation

The average power dissipation in conventional CMOS digital circuit can be classified into three main components

1. The dynamic (switching) power dissipation
2. The short circuit power dissipation and
3. leakage power dissipation.

- * Dynamic power is the power consumed when the device is active when signals of the design are changing values.
- * static power is the power consumed when the device is powered up but no signals are changing value. In CMOS devices, the static power consumption is due to leakage mechanism.

1. Switching power dissipation:-

- * The first and primary source of dynamic power consumption is the switching power dissipation occurs due to the power required to charging and discharging of the output capacitance on a gate.

The energy per transition is given by

$$\text{Energy / Transition} = \frac{1}{2} \times C_L \times V_{DD}^2$$

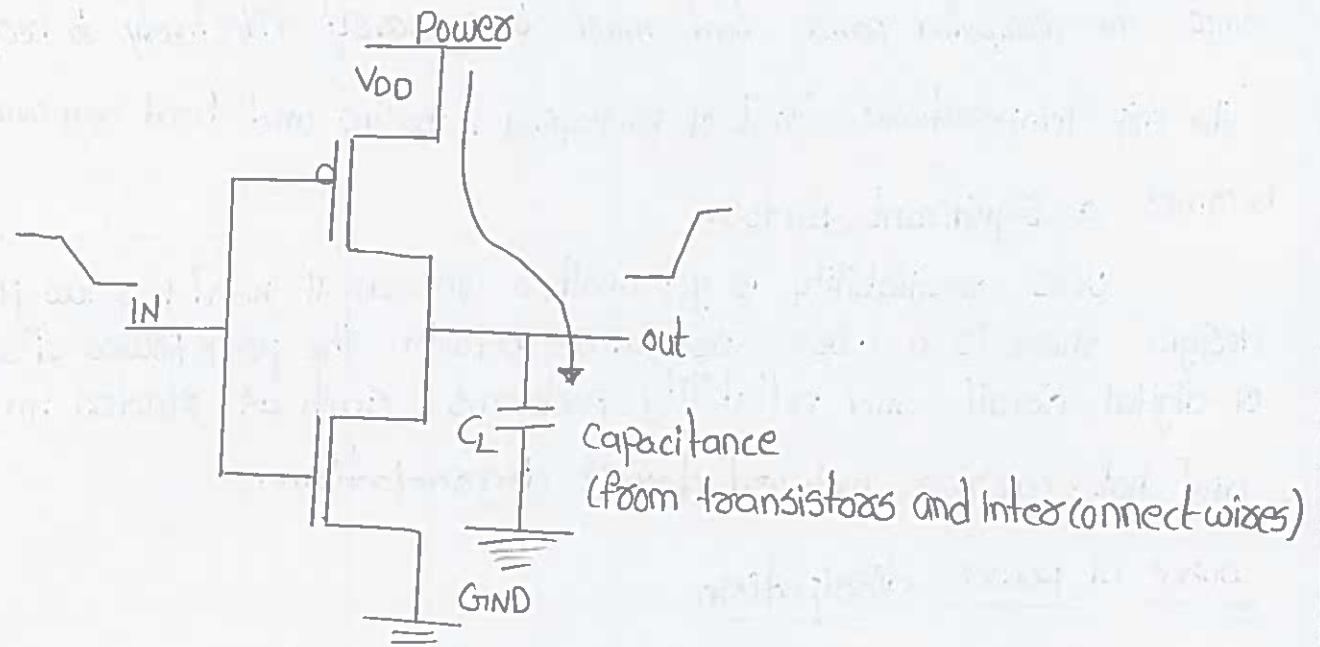


fig:- Dynamic (switching) Power

where C_L is the load capacitance and V_{DD} is the supply voltage. Switching power is therefore expressed as:

$$P_{\text{switch.}} = \frac{\text{Energy}}{\text{Transition}} \times f = C_L \times V_{DD}^2 \times P_{\text{trans.}} \times f_{\text{clock}}$$

where f is the frequency of transition, $P_{\text{trans.}}$ is the probability of output transition and f_{clock} is the frequency of the system clock.

In addition to switching power dissipation for charging and discharging the load capacitance, switching power dissipation also occurs for charging and discharging of the internal node capacitance. Thus total switching power dissipation is given by

$$P_{\text{total switch.}} = C_L \times V_{DD}^2 \times P_{\text{trans.}} \times f_{\text{clock}} + \sum \alpha_i \times c_i \times V_{DD} \times (V_{DD} - V_{th}) \times f_{\text{clock}}$$

where α_i and c_i are the transition probability and capacitance, respectively for an internal node i .

short circuit power dissipation

In addition to switching power, short-circuited power also contributes to dynamic power.

(3)

illustrates shoot - circuit current. shoot - circuit current occurs when both the negative , metal - oxide semiconductor (NMOS) and positive metal - oxide - Semiconductor (PMOS) Transistors are on. Then threshold voltage of NMOS transistor and V_{tp} is the threshold voltage of the PMOS transistor. Then, the period when the voltage value is between V_{tn} and $V_{dd} - V_{tp}$ while input switch either from 1 to 0 or vice versa both the PMOS and the NMOS transistor remain on and shoot circuit current flow from V_{dd} to ground (GND).

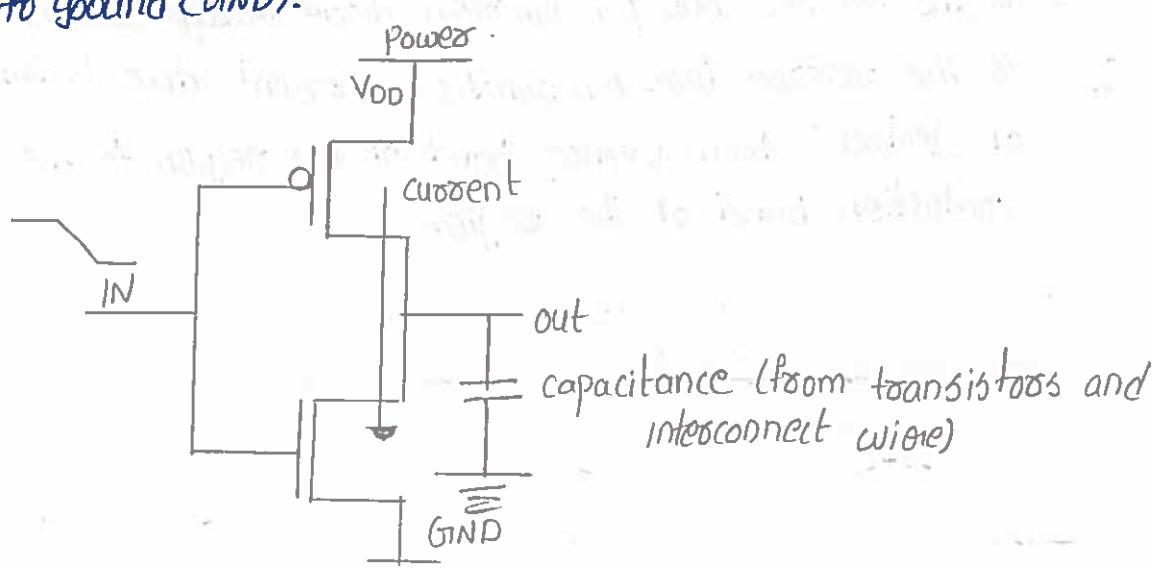


fig:- shoot - circuit current or crowbar current.

The expression for shoot - circuit power is given by

$$P_{\text{shootcircuit}} = t_{\text{sc}} \times V_{dd} \times I_{\text{peak}} \times f_{\text{clock}} = \frac{\mu E_{ox} W}{18 L D} \times (V_{dd} - V_{th})^3 \times t_{\text{sc}} \times f_{\text{clock}}$$

- * where t_{sc} is the rise/fall time duration on the shoot - circuit current
- * I_{peak} is the total internal switching current (shoot - circuit current plus the current to charge the internal capacitance)
- * μ is the mobility of the charge carriers
- * E_{ox} is the permittivity of the silicon dioxide
- * W is width
- * L is length
- * D is the thickness of the silicon dioxide

From the above equation, it is evident that the shoot - circuit power dissipation depends on the supply voltage.

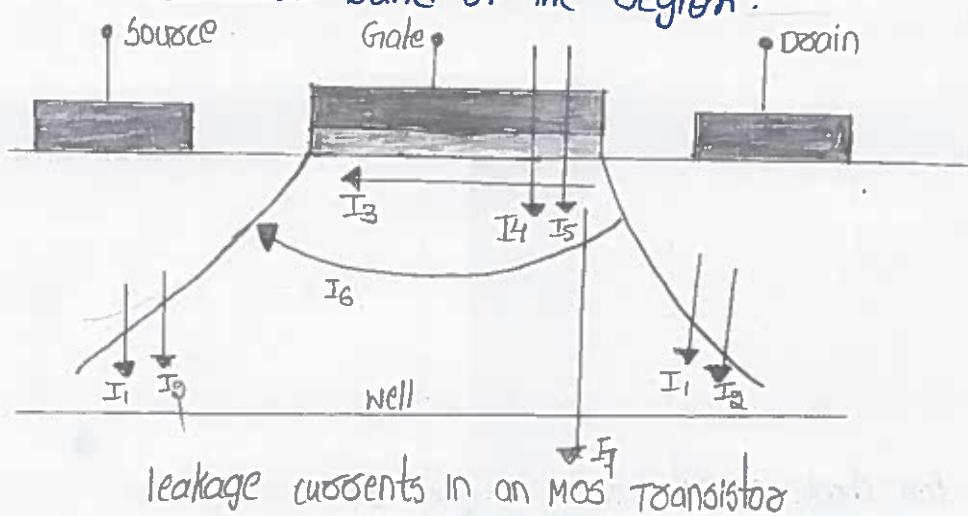
rise/fall time of the input and the clock frequency apart from the physical parameters.. so the short-circuit power can be kept low if the comp. rise/fall time of the input signal, is short for each transition. then, the overall dynamic power is determined by the switching power.

* Static Power Dissipation:-

Static power is the power consumed when the device is powered up but to leakage mechanism.

Here I_1 - is the reverse bias p-n junction diode leakage current.

I_2 - is the reverse bias p-n junction current due to tunneling of electrons from valence band of the region to the conduction band of the region.



leakage currents in an MOS Transistor

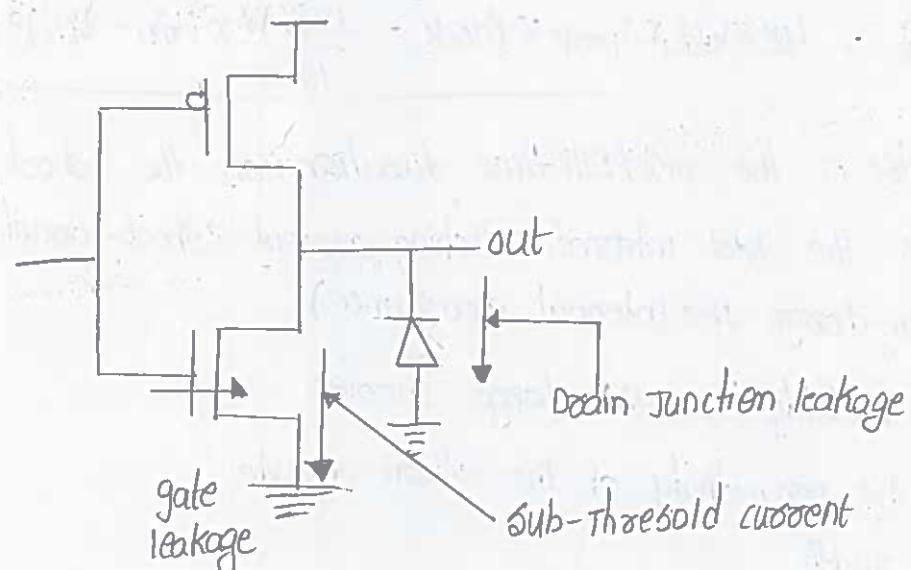


fig:- Leakage currents in a CMOS inverter

A part from these four primary leakages, there are few other leakages current which is also contribute to static power dissipation

- 1) Gate leakage
- 2) Gate induced drain leakage.
- 3) Junction leakage.
- 4) Sub-threshold leakage.

* Reverse-bias p-n junction diode leakage current.

* Hot carrier injection gate current.

* Channel punch through current.

The NMOS and PMOS transistors used in CMOS logic gate generally have non-zero reverse leakage and sub threshold current.

In CMOS VLSI chip, containing a very large number of transistors, these current can contribute to all overall power dissipation.

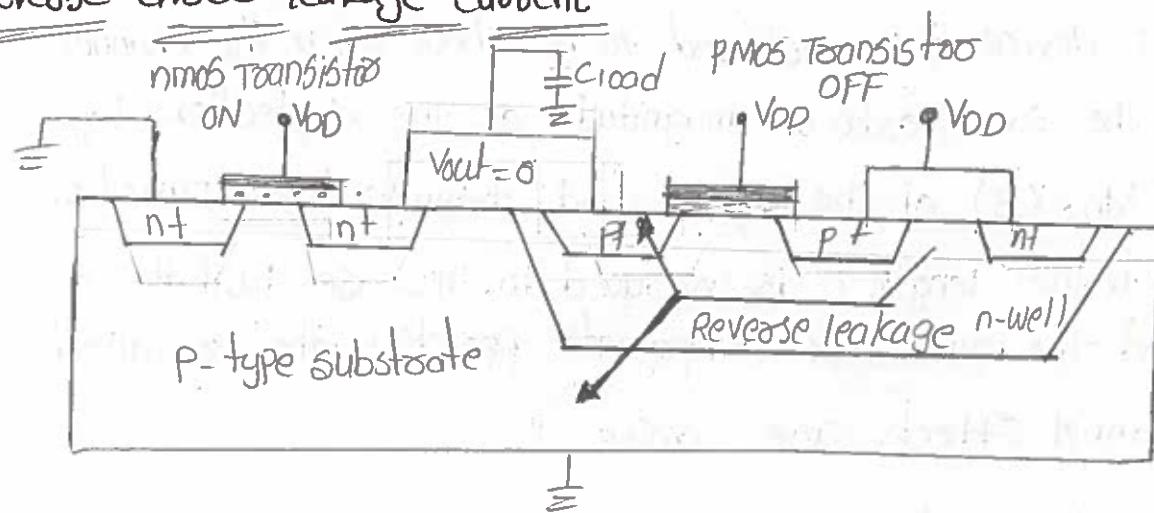
The magnitude of the leakage current is mainly determined by the processing parameters.

The two main leakage current components found in a MOSFET

(1) Reverse diode leakage current

(2) Sub threshold leakage current.

Reverse diode leakage current:



$$I_{reverse} = A \cdot J_0 \left[e^{\frac{qV_{bias}}{kT}} - 1 \right]$$

* Glitching Power dissipation

The third type of dynamic power dissipation is the glitching power which arises due to finite delay of the gates. Since the dynamic power is directly proportional to the number of the output transitions of a logic gate, glitching can be a significant source of signal activity and deserves mention here.

- Glitches often occur when paths with unequal propagation delay converge at the same point in the CKT.
- Glitches occur because the input signal to a particular logic block arrive at different times, causing a no. of intermediate transitions to occur before the output of the logic block stabilizes.
- These additional transitions result in power dissipation which (character) is categorized as the glitching power.

short channel effects

short channel devices:-

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{d0}, x_{ds}) of the source and drain(junction) junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects are arise.

short - channel effects

The short-channel effects are attributes to two physical phenomena:

1. the limitation imposed on electron drift characteristic in the channel
2. the modification of the threshold voltage due to the shortening channel length.

In particular 5 different short-channel effects can be distinguished

1. drain-induced barrier lowering and punch through.
2. surface scattering
3. velocity saturation
4. impact ionization
5. hot electron effect

1. drain-induced barrier lowering and punch through.

The expression for the drain and source junction widths are.

$$x_{d0} = \sqrt{\left[\frac{2\varepsilon_{si}}{qN_A} \right] (V_{DS} + \phi_{Bi} + V_{SB})}$$

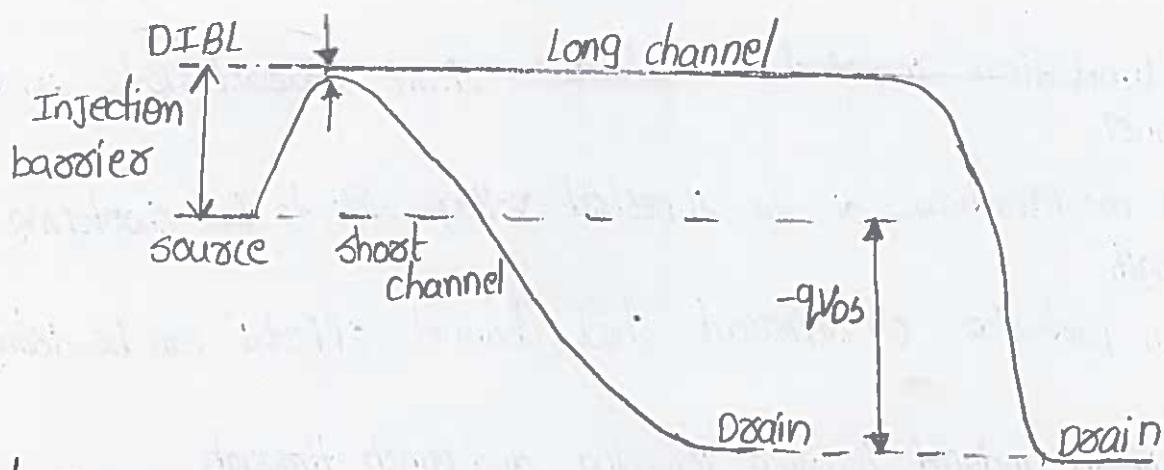
And

$$x_{s0} = \sqrt{\left[\frac{2\varepsilon_{si}}{qN_A} \right] (\phi_{Bi} + V_{DB})}$$

where V_{SB} and V_{DB} are source-to-body and drain-to-body voltages.

There exists a potential barrier between source and drain which is to be lowered by applying gate voltage. In short channel devices in addition to gate voltage, drain voltage also has a significant coupled, so the drain bias can effect the potential barrier to carrier flow through the source junction. sub threshold increases linearly.

As drain depletion region continues to increase with the bias, the source to channel junction & hence lower potential barriers known as DLBI

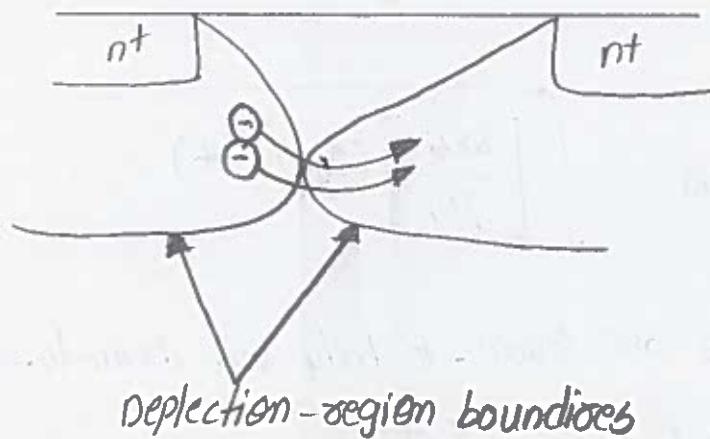


Punch through:

when the drain is at high enough voltage with respect to the source
the depletion region around the drain may extend to the source,
causing current to flow irrespective of gate voltage (i.e even if gate voltage
is zero) this is known as substrate punch through

so when channel length L decreases (i.e short channel gate length case) punch through voltage rapidly decreases.

the depletion region at the drain-substrate and source substrate junctions extend into the channel.

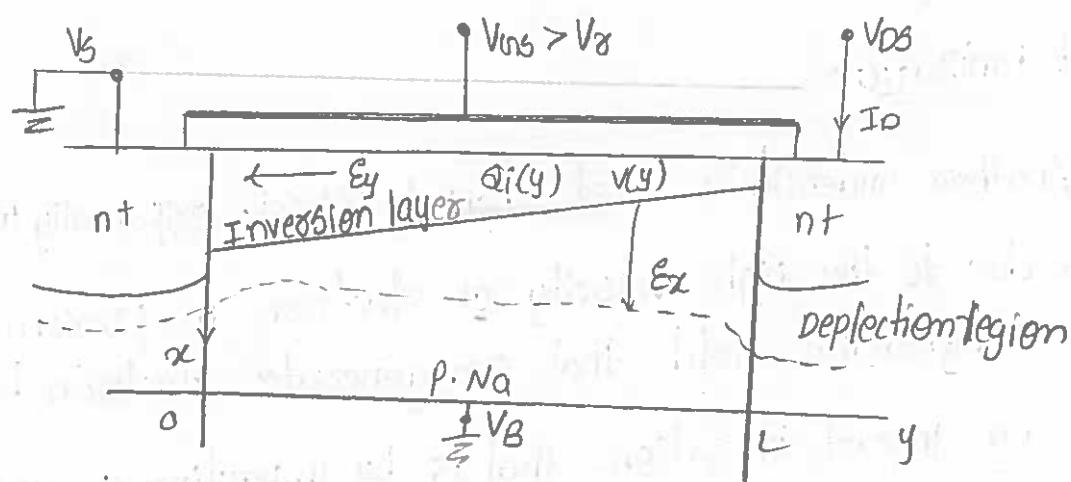


As the channel length is reduced. If the doping is kept constant-
the separation the depletion region boundaries decreases

2. Surface scattering :-

As the channel length become small due to the lateral extension
of the depletion layer into the channel region, the longitudinal
electroic effect field component E_y increases. And the surface

mobility becomes field-dependent. since the carrier transport in a MOSFET is confined within the narrow inversion layer



The surface scattering causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so the average surface mobility even for small values of E_y is about half as much as that of the bulk mobility

3. velocity saturation

The performance short-channel devices are also effected by the velocity saturation, which reduces the transconductance in the saturation mode.

At the low E_y the electron drift velocity V_{de} in the channel varies linearly with the electric field intensity. However, as E_y increases above 10^4 V/cm, the drift velocity tends to increase more slowly, and approaches a saturation value of $V_{de}(\text{sat}) = 10^7$ cm/s around $E_y = 105$ V/cm at 300K

Note that the drain current is limited by velocity saturation instead of pinchoff. This occurs in short channel device when the dimensions are scaled without lowering the bias voltage, using $V_{de}(\text{sat})$, the maximum gain possible for a MOSFET can be defined as

$$g_m = W C_{ox} V_{de} (\text{Sat})$$

4. Impact ionization

Another undesirable short-channel effect, especially in NMOS occur due to the high velocity of electron in presence of high longitudinal field that can generate electron-hole (e-h) pairs by impact ionization. that is by impacting on silicon atoms and ionizing them.

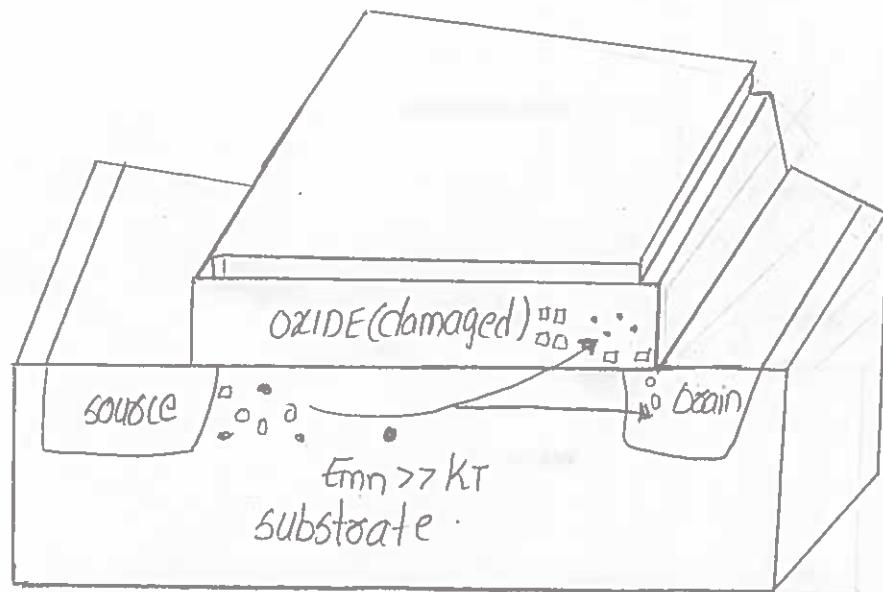
It happens to follow:- normally, most of electrons are attached by drain, while the holes enter the substrate to form part of parasitic substrate current. If the aforementioned holes are collected by the source, and the corresponding holes current creates a voltage drop in the substrate metallization of the order of 0.6V. the normally reversed-biased substrate-source pn junction will conduct appreciably. The electrons can be injected from source to the substrate, similar to the injection electrons from emitted to the base. They can gain enough energy as they travel toward the drain to create new electron hole pairs. If electrons are generated due to high field escape the drain field to travel into the substrate, thereby affecting other devices on chip.

5. Hot electron effect

Another problem related to high electric field is caused by so-called hot electrons.

These high energy electrons can enter the oxide where they can be trapped, giving rise to oxide.

charging that can accumulate with time and degrade the device performance by increasing V_t and affect



Adversely the gate's control on the drain current.

changes to our culture will make us better prepared
to live longer, healthier lives.

It's time to start taking steps to protect